1. Compare super pipeline and superscalar pipelined architecture.

2. What are the difference factors that can affect the performance of a pipelined system?

3. How do you speed up memory access in case of vector processing?
   With architecture and timing diagram explain S-access memory organization.

4. What is pipelining?

Consider the following reservation table:

```
   1   2   3   4
S1  x   x   x
S2  x   x   
S3  x   
```

Write down the

a. Forbidden latency.

b. Initial collision vector.
c. Draw the state diagram for scheduling the pipeline.

d. Find out the Greedy cycle and MAL.

e. If the pipeline clock state is 25MHz, then what is the throughput of the pipeline?

f. What are the bounds on MAL?

**Advanced Computer Architecture**

**CS-403**

**Group-b**

1. Consider the five stage pipelined processor specified by the following reservation table.

<table>
<thead>
<tr>
<th></th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
</tr>
</thead>
<tbody>
<tr>
<td>S1</td>
<td>x</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>x</td>
</tr>
<tr>
<td>S2</td>
<td>x</td>
<td></td>
<td></td>
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<td>x</td>
<td></td>
</tr>
<tr>
<td>S3</td>
<td></td>
<td>x</td>
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<td></td>
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<td></td>
</tr>
<tr>
<td>S4</td>
<td></td>
<td></td>
<td>x</td>
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<tr>
<td>S5</td>
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<td></td>
<td></td>
<td>x</td>
<td></td>
<td>x</td>
</tr>
</tbody>
</table>

a. What are the forbidden latencies and the initial collision vector?

b. Draw the state transition diagram for scheduling the pipeline.

c. Determine all simple cycles, greedy cycles and MAL.

d. What will be the maximum throughput of the pipeline?

2. What is meant by horizontal and vertical vector processing? Find out speed up of vertical vector processing over uniprocessing.
3. What is vector processor? What do you mean by pipelined chaining?


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**Advanced Computer Architecture**

**CS-403**

**Group-c**

1. Discuss about strip mining and vector stride in vector processors.

2. Draw the block diagram of C-access memory function. Why is it necessary and how does it improve the memory access time?

3. What is vector processor? Give the block diagram to indicate the architecture of a typical Vector Processor with multiple function pipes.

4. Write short notes on:
   
   e. Reservation table.
   
   f. Memory to memory vector architecture.
   
   g. Scalar and Vector processor.
h. Pipeline hazards.

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*Advanced Computer Architecture*

*CS-403*

*Group-d*

1. Define speedup and throughput of a parallel processing system.

2. Give the classification of the Vector instruction.
i. Indicate the different fields by which Vector instructions are usually specified.

ii. Give the block diagram to indicate the architecture of a typical Vector Processor with multiple function pipes.

3. Discuss the advantage of vector processor over scalar processor.

4. Assume a four stage pipeline:

j. Fetch: Read the instruction from memory.

k. Decode: Decode the instruction.

l. Execute: Execute the instruction.

m. Write: Store the result in destination location.

Assume a job consists of 6 tasks.

Draw the space-time diagram for pipeline.
1. Consider the five stage pipelined processor specified by the following reservation table.

<table>
<thead>
<tr>
<th></th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
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<tbody>
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<td>S5</td>
<td>x</td>
<td></td>
<td></td>
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<td>x</td>
</tr>
</tbody>
</table>

n. What are the forbidden latencies and the initial collision vector?

o. Draw the state transition diagram for scheduling the pipeline.

p. Determine all simple cycles, greedy cycles and MAL.

q. What will be the maximum throughput of the pipeline?

2. What are the difference factors that can affect the performance of a pipelined system?

Differentiate between WAR and RAW with a suitable example

3. How do you speed up memory access in case of vector processing?

With architecture and timing diagram explain S-access memory organization.
4. I. Compare super scalar, super-pipeline and VLIW technique.
   
   ii. Compare Memory to memory vector architecture and register to register architecture.

   Advanced Computer Architecture

   CS-403

   Group-f

1. Define speedup and throughput of a parallel processing system.

2.
   i. Give the classification of the Vector instruction.
   
   ii. Indicate the different fields by which Vector instructions are usually specified.
   
   iii. Give the block diagram to indicate the architecture of a typical Vector Processor with multiple function pipes.

3. I. Compare super scalar, super-pipeline and VLIW technique.
   
   ii. Describe c/s-access memory organization.

4. Assume a four stage pipeline:
   
   r. Fetch: Read the instruction from memory.
   
   s. Decode: Decode the instruction.
   
   t. Execute: Execute the instruction.
u. **Write:** Store the result in destination location.

Assume a job consists of 6 tasks.

Draw the space-time diagram for pipeline.